IN THE SPECIFICATION

1. Please amend paragraph [0044] as follows:

[0044] FIGURE 2 illustrates a block diagram that represents a typical prior art frequency multiplier (Fmul) type of a clock generator. It comprises a high frequency pulse train generator (HFPG) 21, a frequency control logic 23, a reference clock counter (RCC) 22, a high-frequency clock counter (HFCC) 24 and a comparator 27, all interconnected as shown in FIGURE 2. RCC 22 receives a reference clock and a window count value N. Comparator [[26]] 27 receives, as a comparison value, a nominal high frequency count value M. In operation, RCC 22 counts a number of successive reference clock pulses equal to the given window count N and outputs a reference window signal over the duration of this counting. The reference window signal is applied to HFCC 24, which counts successive pulses in the high frequency clock, output by HFPG 21, over the duration of the reference window. The count from the HFCC is applied to comparator 27 which compares it with M. As a result, the comparator outputs a by-level signal indicating whether the count exceeds M or is less than M. This signal is applied to frequency control logic 23 which accordingly corrects the frequency control value that it continuously sends to ~~pulse train generator~~ HFPG 21. This operational cycle is repeated indefinitely.

2. Please amend paragraph [0047] as follows:

[0047] Yet another type of possible malfunction, for which monitoring is desirable, is associated with the control mechanism in the HFPG. The control value obtained from control logic [[22]] 23 is transmitted as a digital signal and is converted within HFPG 21 to an analog signal by means of a digital-to-analog converter (D/A). Inherent inaccuracies in the D/A may cause the differences between certain adjacent value levels to be different from others, thus possibly causing appreciable jumps in the frequency during the correction process.